WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit comprising:

circuits having a certain function;

a plurality of input terminals which receive input data to said circuits from the outside;

a plurality of output terminals which output data output from said circuits to the outside;

a plurality of first registers connected in series, said plurality of first registers shifting stored data to respective adjacent registers in sequence, and said plurality of first registers being connected in one-to-one correspondence to said plurality of input terminals or to said plurality of output terminals;

a plurality of second registers connected in series, said plurality of second registers shifting stored data to respective adjacent registers in sequence, and said plurality of second registers being connected in one-to-one correspondence to said plurality of input terminals or to said plurality of output terminals;

a first scan input terminal formed at one end of said plurality of first series-connected registers;

a first scan output terminal formed at the other end of said plurality of first series-connected registers;

a second scan input terminal formed at one end of

said plurality of second series-connected registers;

a second scan output terminal formed at the other end of said plurality of second series-connected registers; and

an operation control circuit which controls operations of said circuits and said plurality of first and second registers.

2. The semiconductor integrated circuit according to claim 1, wherein said first scan output terminal and said second scan input terminal are arranged adjacent to each other in the same end portion, and said semiconductor integrated circuit further comprises a line formed between said first scan output terminal and said second scan input terminal.

3. The semiconductor integrated circuit according to claim 1, wherein

said operation control circuit comprises:

a plurality of third and fourth registers connected to input and output terminals;

a third scan input terminal connected to one end of said plurality of third registers;

a third scan output terminal connected to the other end of said plurality of third registers;

a fourth scan input terminal connected to one end of said plurality of fourth registers; and

a fourth scan output terminal connected to the other end of said plurality of fourth registers,

said third scan input terminal is connected to said first scan output terminal, and said fourth scan output terminal is connected to said second scan input terminal.

4. The semiconductor integrated circuit according to claim 3, wherein said third scan output terminal and said fourth scan input terminal are arranged adjacent to each other at the same end portion, and said semiconductor integrated circuit further comprises a line formed between said third scan output terminal and said fourth scan input terminal.

5. The semiconductor integrated circuit according to claim 1, wherein said circuits, said plurality of input terminals, said plurality of output terminals, said plurality of first and second registers, said first scan input terminal, said first scan output terminal, said second scan input terminal, and said second scan output terminal configure a first integrated circuit, said operation control circuit is placed adjacent to said first integrated circuit, and a second integrated circuit having an arrangement which is the mirror inversion of said first integrated circuit is placed on a side of said operation control circuit away from the side at which said first integrated circuit is formed.

6. The semiconductor integrated circuit according to claim 1, wherein said circuits comprise:

a memory cell array in which a plurality of memory cells are arrayed in row and column directions;

a row decoder which selects said memory cells arrayed in the row direction;

a column decoder which selects said memory cells arrayed in the column direction; and

a sense amplifier which reads out data from a selected memory cell.

7. A semiconductor integrated circuit comprising:

circuits having a certain function;

a plurality of input terminals which receive input data to said circuits from the outside;

a plurality of output terminals which output data output from said circuits to the outside;

a plurality of first registers connected in series, said plurality of first registers shifting stored data to respective adjacent registers in sequence, and said plurality of first registers being connected in one-to-one correspondence to said plurality of input terminals and said plurality of output terminals;

a plurality of buffers connected in series, said plurality of buffers amplifying data;

a first scan input terminal formed at one end of said plurality of first series-connected registers;

a first scan output terminal formed at the other end of said plurality of first series-connected

registers;

a second scan input terminal formed at one end of said plurality of series-connected buffers;

a second scan output terminal formed at the other end of said plurality of series-connected buffers; and

an operation control circuit which controls operations of said circuits and said plurality of first registers.

8. The semiconductor integrated circuit according to claim 7, wherein said first scan output terminal and said second scan input terminal are arranged adjacent to each other in the same end portion, and said semiconductor integrated circuit further comprises a line formed between said first scan output terminal and said second scan input terminal.

9. The semiconductor integrated circuit according to claim 7, wherein

said operation control circuit comprises:

a plurality of second and third registers connected to input and output terminals;

a third scan input terminal connected to one end of said plurality of second registers;

a third scan output terminal connected to the other end of said plurality of second registers;

a fourth scan input terminal connected to one end of said plurality of third registers; and

a fourth scan output terminal connected to the

other end of said plurality of third registers,

said third scan input terminal is connected to said first scan output terminal, and said fourth scan output terminal is connected to said second scan input terminal.

10. The semiconductor integrated circuit according to claim 9, wherein said third scan output terminal and said fourth scan input terminal are arranged adjacent to each other in the same end portion, and said semiconductor integrated circuit further comprises a line formed between said third scan output terminal and said fourth scan input terminal.

11. The semiconductor integrated circuit according to claim 7, wherein said circuits, said plurality of input terminals, said plurality of output terminals, said plurality of first registers, said plurality of buffers, said first scan input terminal, said first scan output terminal, said second scan input terminal, and said second scan output terminal configure a first integrated circuit, said operation control circuit is placed adjacent to said first integrated circuit, and a second integrated circuit having an arrangement which is the mirror inversion of said first integrated circuit is placed on a side of said operation control circuit away from the side at which said first integrated circuit is formed.

12. The semiconductor integrated circuit according

to claim 7, wherein said circuits comprise:

a memory cell array in which a plurality of memory cells are arrayed in row and column directions;

a row decoder which selects said memory cells arrayed in the row direction;

a column decoder which selects said memory cells arrayed in the column direction; and

a sense amplifier which reads out data from a selected memory cell.

13. A semiconductor integrated circuit comprising:

circuits having a certain function;

a plurality of input terminals which receive input data to said circuits from the outside;

a plurality of output terminals which output data output from said circuits to the outside;

a plurality of first registers connected in series, said plurality of first registers shifting stored data to respective adjacent registers in sequence, and said plurality of first registers being connected in one-to-one correspondence to said plurality of input terminals or to said plurality of output terminals;

a plurality of second registers connected in series, said plurality of second registers shifting stored data to respective adjacent registers in sequence, and said plurality of second registers being connected in one-to-one correspondence to said

plurality of input terminals or to said plurality of output terminals;

a first scan input terminal formed at one end of said plurality of first series-connected registers;

a first scan output terminal formed at one end of said plurality of second series-connected registers, said first scan output terminal being placed adjacent to said first scan input terminal;

a line formed between the other end of said plurality of first series-connected registers and the other end of said plurality of second series-connected registers; and

an operation control circuit which controls operations of said circuits and said plurality of first and second registers.

14. The semiconductor integrated circuit according to claim 13, wherein

said operation control circuit comprises:

a third scan input terminal to which data is input;

a third scan output terminal connected to said third scan input terminal;

a plurality of third registers connected to input and output terminals;

a fourth scan input terminal connected to one end of said plurality of third registers; and

a fourth scan output terminal connected to the

other end of said plurality of third registers,

said third scan output terminal is connected to said first scan input terminal, and said fourth scan input terminal is connected to said first scan output terminal.

15. The semiconductor integrated circuit according to claim 13, wherein said circuits, said plurality of input terminals, said plurality of output terminals, said plurality of first and second registers, said first scan input terminal, said first scan output terminal, and said line configure a first integrated circuit, said operation control circuit is placed adjacent to said first integrated circuit, and a second integrated circuit having an arrangement which is the mirror inversion of said first integrated circuit is placed on a side of said operation control circuit away from the side at which said first integrated circuit is formed.

16. The semiconductor integrated circuit according to claim 13, wherein said circuits comprise:

a memory cell array in which a plurality of memory cells are arrayed in row and column directions;

a row decoder which selects said memory cells arrayed in the row direction;

a column decoder which selects said memory cells arrayed in the column direction; and

a sense amplifier which reads out data from a

selected memory cell.

17. A semiconductor integrated circuit comprising:

circuits having a certain function;

a plurality of input terminals which receive input data to said circuits from the outside;

a plurality of output terminals which output data output from said circuits to the outside;

a plurality of first registers connected in series, said plurality of first registers shifting stored data to respective adjacent registers in sequence, and said plurality of first registers being connected in one-to-one correspondence to said plurality of input terminals and said plurality of output terminals;

a plurality of first buffers connected in series, said plurality of first buffers amplifying data;

a first scan input terminal formed at one end of said plurality of first series-connected registers;

a first scan output terminal formed at the other end of said plurality of first series-connected registers;

a second scan input terminal formed at one end of said plurality of first series-connected buffers;

a second scan output terminal formed at the other end of said plurality of first series-connected buffers;

an operation control circuit which outputs a clock

signal for controlling a data shift operation of said plurality of first registers; and

a plurality of second buffers which delay the clock signal output from said operation control circuit and supply the delayed clock signal to said plurality of first registers.

18. The semiconductor integrated circuit according to claim 17, wherein

said operation control circuit comprises:

a plurality of second and third registers connected to input and output terminals;

a third scan input terminal connected to one end of said plurality of second registers;

a third scan output terminal connected to the other end of said plurality of second registers;

a fourth scan input terminal connected to one end of said plurality of third registers; and

a fourth scan output terminal connected to the other end of said plurality of third registers,

said third scan input terminal is connected to said first scan output terminal, and said fourth scan output terminal is connected to said second scan input terminal.

19. The semiconductor integrated circuit according to claim 17, wherein said circuits, said plurality of input terminals, said plurality of output terminals, said plurality of first registers, said plurality of

first buffers, said plurality of second buffers, said first scan input terminal, said first scan output terminal, said second scan input terminal, and said second scan output terminal configure a first integrated circuit, said operation control circuit is placed adjacent to said first integrated circuit, and a second integrated circuit having an arrangement which is the mirror inversion of said first integrated circuit is placed on a side of said operation control circuit away from the side at which said first integrated circuit is formed.

20. The semiconductor integrated circuit according to claim 17, wherein said circuits comprise:

a memory cell array in which a plurality of memory cells are arrayed in row and column directions;

a row decoder which selects said memory cells arrayed in the row direction;

a column decoder which selects said memory cells arrayed in the column direction; and

a sense amplifier which reads out data from a selected memory cell.